SoC Workshop
Developing with Intel® ARM®-based SoCs

Course Description

This course is intended for hardware and firmware engineers and will leverage your knowledge of Qsys system design to guide you on implementing an Altera SoC with the ARM Cortex A9 hard processing system (HPS). This course covers the hardware aspects of using the processor in the SoC from the design, verification and debug hardware perspectives just as if the processor was external. Our intention is that you feel completely comfortable using the HPS in the SoC and know all of the resources at your disposal to work with the board designer, FPGA engineer, firmware engineer or software engineer to get up and running quickly.
The software part of this course is intended to teach you about SoC software bringup and development. The course isn't intended to teach you software application or driver development, but rather concentrates on the unique aspects of the embedded HPS software flow in an SoC. You'll learn everything you need to know to get started developing your software for the HPS component right away, where to go to get help, as well as how to use the Altera edition of the ARM DS-5 adaptive debugging tools at your disposal to debug your software.

Agenda

- Create, manage, and compile an SoC in the Qsys tool
- Simulate the HPS component as part of a Qsys system using Mentor Graphics ModelSim® tool
- Bring up and debug an SoC with the System Console tool
- Cross trigger between the FPGA and ARM processors using the SignalTap II logic analyzer
- Understand the hardware to software file handoff
- Design with the Golden reference design on the Cyclone V SoC development kit
- Understand the stages in the HPS boot sequence & the boot scenarios
- Create a preloader & baremetal application to walkthrough the booting & configuring the HPS & blink an LED in the SoC
- Get started with a variety of OSs for the ARM processor
- Use the community portal to get the Yocto Linux distribution, find help from other developers, & get started with development kits
- Use DS-5 software to develop & debug an ARM-based application

Skills Required

- FPGA, Quartus or Platform Designer/Qsys knowledge is not required, but a plus
- Some basic software knowledge and basic C/C++ coding skills

Exercises

- Creating an ARM Based SoC System Using Platform Designer/Qsys
- Exercise the FPGA Using the System Console Tool
- Debugging Hardware using SignalTapTM II Logic Analyzer
- Creating the Preloader for an ARM Based SoC
- Creating and Debugging a Baremetal System for an ARM Based SoC with HWLibs
- Boot and Add Linux App
- Cross Triggering and Debug

Course Length	2 days
Language	Presentation in German or English and documentation in English
Platform	PC Windows 10
Pricing	Public: 1550,- EUR / attendee In-House: On Request
Dates	See schedule at elcamino.de

Intel® FPGA Technical Training

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