System Integration with Platform Designer (fka Qsys)

Course Description

This class will teach you how to quickly build designs for Intel® FPGAs using Intel's Platform Designer system-level integration tool. You will become proficient with Platform Designer and will expand your knowledge of the Quartus Prime FPGA design software. You will learn how to build hierarchical systems quickly by integrating IP and custom logic and also how to optimize designs for performance. Since Platform Designer makes design reuse easy through standard interfaces, we will dive deep into the Avalon-Memory Mapped and Streaming Interfaces. The class provides a significant hands-on component, where you will gain deep exposure to tool usage as well as system and custom HDL component design.

Agenda

- Utilize key features of Platform Designer, understand the files & how they fit into the Quartus Prime project hierarchy
- Build electronic systems with Platform Designer
- Exploit Platform Designers' hierarchical capability to add flexibility & scalability to your design
- Test systems using ModelSim
- Create custom components with Avalon-MM or Avalon-ST interfaces
- Test custom components with Avalon Verification Suite or BFMs
- Perform in-system diagnosis & control via System Console
- Integrate CPU subsystems into a project

Skills Required

- FPGA, Quartus Prime or Platform Designer knowledge is not required, but a plus
- Some basic software knowledge and basic C/C++ coding skills is not required, but a plus

Exercises

- Introduction to Platform Designer
- Implement a PCI Express endpoint using Platform Designer in a Cyclone IV GX device
- Build a Data Path Hardware System in Platform Designer that Incorporates Custom Logic
- Add a Control Plane to the Design and Test the System
- Testing Custom Components with BFMs
- Testing the System with BFMs
- Testing the System with System Console
- Platform DesignerHierarchy
  - Expand system to support four parallel video processing channels
  - Run the four-channel system under Nios II software control

Course Length	2 days
Language	Presentation in German or English and documentation in English
Platform	PC Windows 10
Pricing	Public: 1550,- EUR / attendee In-House: On Request
Dates	See schedule at elcamino.de

Intel® FPGA Technical Training

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