Intel® Quartus® Prime Software
Pro Edition Features for High-End Designs

Course Description

In this course, you will learn about new features in the Pro Edition software to help you plan, implement, and close timing when using Intel Arria® 10 and Stratix® 10 FPGAs. You will learn how to migrate a design to the Intel Quartus Prime Pro Edition software from the standard edition, or plan a new design from scratch using the Interface Planner. You will learn how to take advantage of new compilation flow stages and incremental optimization for faster design compiles. You will learn how to use block-based design to ease team-based design work and to take advantage of partial reconfiguration. New features for timing analysis will be covered including the clock domain crossing (CDC) viewer. A scripted flow for the tools will be emphasized throughout the course, including the labs.

Agenda

- Plan a design using the Interface Planner & Logic Lock regions
- Use incremental optimization stages such as post-place physical synthesis & post-route fix-up to increase performance
- Describe the steps needed to implement partial reconfiguration
- Understand the Pro Edition software timing reports
- Evaluate the sufficiency of clock crossing logic using the CDC Viewer
- Understand command-line & TCL scripting interfaces available in the Pro Edition software & learn to use them

Skills Required

- The Quartus Prime Software: Foundation class or familiarity with the Intel Quartus Prime software
- Familiarity with Verilog or VHDL synthesizable design structures
- Familiarity with timing constraint concepts

Exercises

- Migrate a Design and Perform Early Design Planning
- Use Block-Based Design Methodology
- Examine the New Features in the Timing Analyzer
- Scripting and Automating

Course Length	1 day
Language	Presentation in German or English and documentation in English
Platform	PC Windows 10
Pricing	Public: 800,- EUR / attendee In-House: On Request
Dates	See schedule at elcamino.de

Intel® FPGA Technical Training

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