e8254 Timer

Programmable Interval Timer

Functional Description

The e8254 is a synchronous implementation of the industry standard 8254 counter/timer, which is designed to solve the timing control problems common in microcomputer system design. It provides up to three independent 16-bit counters, each capable of handling clock inputs up to half the system clock frequency. The implementation is fully software compatible with the original 8254 programmable interval timer.

Features of the original 8254

- Three independent 16-bit counters
- Six programmable counter modes
  - Mode 0: Interrupt on Terminal Count
  - Mode 1: Hardware Retriggerable One-Shot
  - Mode 2: Rate Generator
  - Mode 3: Square Wave Mode
  - Mode 4: Software Triggered Strobe
  - Mode 5: Hardware Triggered Strobe
- Binary or BCD counting
- Reading the counters and status:
  - Simple read operations
  - Latch command
  - Read-back command
- Read/Write LSB/MSB only or LSB first then MSB

Additional e8254 Features

- Developed in Verilog (source code license available)
- Fully synchronous implementation (additional master CLK input)
- GATE and CLKx inputs sampled with master CLK
- Synchronous, registered and glitch free OUTx generation
- Synchronous processor interface
- Defined state after reset for all internal registers and outputs (additional RST_ input)
- Optional fixed counter modes to save resources
- Optional fixed binary counting or fixed BCD counting to save resources

Applications

The e8254 is ideal for integrating existing 8254 based designs. There's no need to touch existing code due to the 100% software compatibility. On the other hand the synchronous character of the core allows reliable and easy to manage implementations in both programmable logic and ASIC technologies. Through parameterization either the full functionality ore only the required modes of the counters can be implemented which gives an optimal utilization.

Deliverables

- Encrypted gate level netlist optimized for Altera's FPGA architectures
- Verilog testbench

alternative

- Verilog source code
- Verilog testbench

Architecture Specification

Coding Style

The circuit is clocked by a single master clock. All other signals are synchronous to the master clock. Asynchronous inputs are synchronized. There are no gates within the clock path and there is only one global asynchronous reset. No use of transparent latches etc.

Variations to the 82C54 Timer Specification

- **Additional Signal CLK**
  This is the master clock of the circuit. There is only the positive clock edge used. All other signals are synchronous to the master clock or are synchronized. The maximum frequency is at least 20 MHz, depending on the target device.

- **Additional Signal RST_**
  There is a global, asynchronous, low active reset signal RST_ to set all signals to a defined initial state.
  The value after reset of the ouput OUTx of the Timer IP-Core is now defined as high. This is in contrast to the original Intel design where the OUT is undefined until a Control Word is written.
  It is recommended that the deassertion of the RST_ signal is synchronized to the system clock externaly to the timer IP-core.

- **Restrictions on the signals CLK0, CLK1, CLK2, GATE0, GATE1, GATE2**
  Please note the difference of the Master Clock CLK and the input signals GATE and CLKx, where x depends on the used counter (i.e. CLK0, CLK1, CLK2). The latter ones are regarded to be no clocks, they are labeled events, which are synchronized with the

rising edge of the master CLK. These signals are assumed to be asynchronous to the clock CLK and are synchronized to the master clock CLK. Thereby are the following restrictions: The maximum frequency is the half of the master clock CLK and the minimum pulse width is one CLK clock cycle.
These signals are asynchronous inputs to the timer/counter. They don't need to meet any setup or hold times.

- **Modification of the local bus interface**
  The local bus interface is now synchronous to the master CLK.

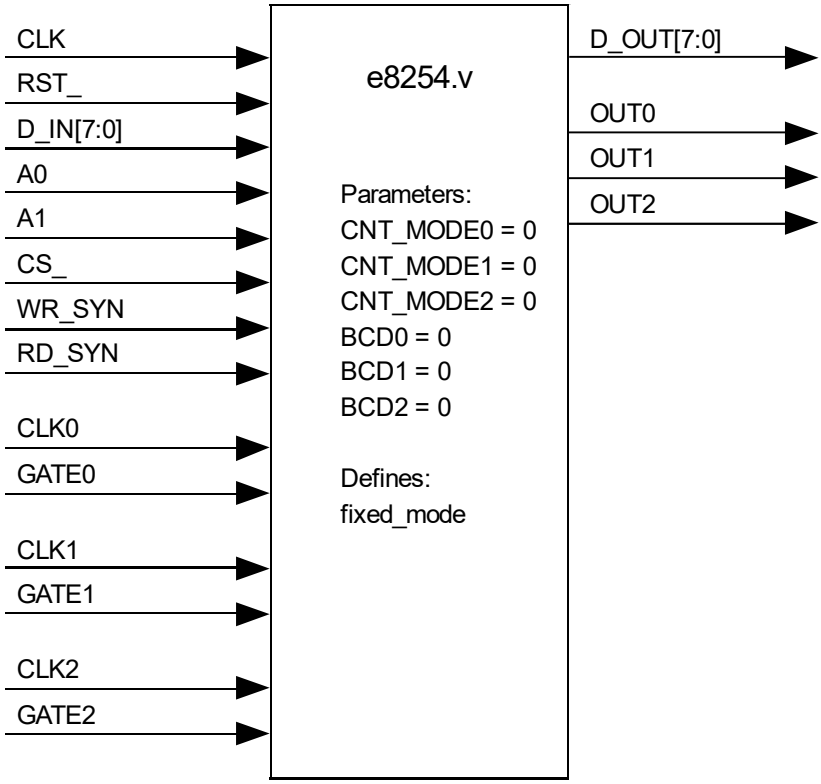
- **Write Signal /WR**
  The asynchronous and low active /WR signal has been changed to the synchronous and high active WR_SYNC signal. This signal is high for one clock cycle during each write-cycle. I.e. a one at the rising edge of the clock CLK triggers a write access if at that time /CS is set to low. The addresses A1 and A0 determine the registers.
  This signal needs to meet setup and hold times relative to the system clock.

- **Read Signal /RD**
  The asynchronous and low active /RD signal has been changed to the synchronous and high active RD_SYNC signal. This signal is high for one clock cycle during each read-cycle. I.e. a one at the rising edge of the clock triggers a read access if at that time /CS is set to low. The addresses A1 and A0 determine the registers selected.
  Thi signal needs to meet setup and hold times relative to the system clock.

- **Addresses A1, A0 and chip select /CS**
  These signals are now synchronous to the master clock CLK and will continue to control the access to the timer IP-core. They need to be valid when WR_SYNC or RD_SYNC are active.
  These signals need to meet setup and hold times relative to the system clock

- **Data Bus [7..0]**
  The bi-directional data bus is splitted into a separate input-bus D_IN[7:0] and an output-bus D_OUT[7:0]. D_IN[7:0] is needed for write operations. D_OUT[7:0] supplies the read-data of the internal registers and is only dependent from the address A1, A0. The input data bus D_IN[7:0] needs to meet setup and hold times relative to the system clock.

IO Ports



Parameters

Fixed Mode versus Variable Mode

In most application all of the three counters will always operate in the same mode 0 to 5 and always use the same binary or BCD counting scheme. In order to save resources it is possible to fix the mode and counting scheme for each individual counter.
By default, when no parameters are passed to the e8254 core it will behave exactly as the original Intel 8254 timer. In this mode the timer IP-core is 100% software compatible to the original discrete timer. Little differences in timing can not be avoided and are due to the synchronous implementation in a different technology.
If „fixed_mode“ is defined in the file „defines.v“ then all three counters in the e8254 cores have a constant mode of operation (0 to 5) and a constant counting scheme (BCD or binary). Any values written into bits D3, D2, D1 and D0 of the Control Word will be ignored. Writing a control word however will otherwise have the same effect as in the fully compatible/variable mode. Reading the control word will return the predefined mode.

When instantiating the e8254 counter the following parameters can be set:

```
e8254_inst  #(CNT_MODE0,CNT_MODE1,CNT_MODE2,
              BCD0,BCD1,BCD2) e8254 (
```

Table 1: e8254 Parameters

Parameter	Legal Values	Default	Description
CND_MODE0	0-5	0	Fixed mode for counter 0
CNT_MODE1	0-5	0	Fixed mode for counter 1
CNT_MODE2	0-5	0	Fixed mode for counter 2
BCD0	0: binary 1: BCD	0	counting scheme for counter 0
BCD1	0: binary 1: BCD	0	counting scheme for counter 1
BCD2	0: binary 1: BCD	0	counting scheme for counter 2

Resource Utilization and Performance

The following results are based on synthesis and place & route in Quartus II Version 4.0. Implementations in other architectures or with other synthesis tools may lead to different results. Contact El Camino for more detailed results on specific target architectures.
The Fmax frequency is the maximum synchronous clock frequency supported. The maximum input clock frequency CLKx to the individual counter has to be below half the actual system clock frequency.
The following results are push-button results without any specific optimization for speed or area.

Table 2: Resources and Performance

Options	Device Family	Logic Elements	Fmax
Variable Mode	MAXII	660	130 MHz
	Cyclone	660	182 MHz
	Stratix	660	187 MHz
Fixed Mode, Default Settings	MAXII	349	138 MHz
	Cyclone	349	256 MHz
	Stratix	349	264 MHz

Notes:

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