General Description

The DIGILAB SX 10 is a universal FPGA prototyping platform based on the Intel® Stratix® 10 device family. It can be used for ASIC prototyping, hardware evaluation or as a verification acceleration vehicle

Features

- Available with Intel Stratix 10 device 1SG280LN3F43E3VG
  - Stratix 10 GX Device Family with 2,753,000 LEs
  - LN3: 24 L-Tile Transceivers, -3 speed grade (not used)
  - F43: 1760 pin, 42.5 x 42.5 mm FineLine BGA package
  - E: Extended Temp Grade (0 – 100°C junction)
  - 3: Core Speed 3
  - V: SmartVID (individual core voltage)
  - G: RoHS6
- 222 user I/Os through
  - Two 40 pin DIL headers
  - Two 38 pin Mictor connectors
  - Two 50 pin Samtec ERF8 connectors
  - Two ETM (Embedded Trace Macrocell) debug connectors
  - JTAG Multi-ICE debug connector
  - Shared test points
- Configuration
  - SD card for non-volatile configuration
  - Optional QSPI Flash for non-volatile configuration
  - Push-buttons for reset and configuration
  - Various LEDs for configuration status
- User Interface
  - 4 x 4 two-state DIP switches
  - 7 push buttons
  - 16 LEDs
  - 4x16 character LCD display
  - Rotary Switch
  - JTAG connector for Altera download cable
- Communication Interfaces
  - Two USB UART interface
  - Two connectors for SPI/I²C interfacing
- Clocking
  - 80 MHz Crystal oscillator
  - 2 SMA clock inputs
- Power supply circuitry with 12V input
- FPGA controlled active heat sink and temperature sensor

Content

Preface

The development board must be stored between -40°C and 85°C. The recommended operating temperature is between 0°C and 70°C. Please contact El Camino for availability information on DIGILAB SX 10 boards that support the industrial temperature range of -40°C to 85°C.

The board can be damaged without proper anti-static handling. Anti-static precautions should be taken before handling the board.

Overview

The DIGILAB SX 10 is a universal FPGA prototyping platform based on Altera's Stratix® 10 device family. It can be used for ASIC prototyping, hardware evaluation or as a verification acceleration vehicle

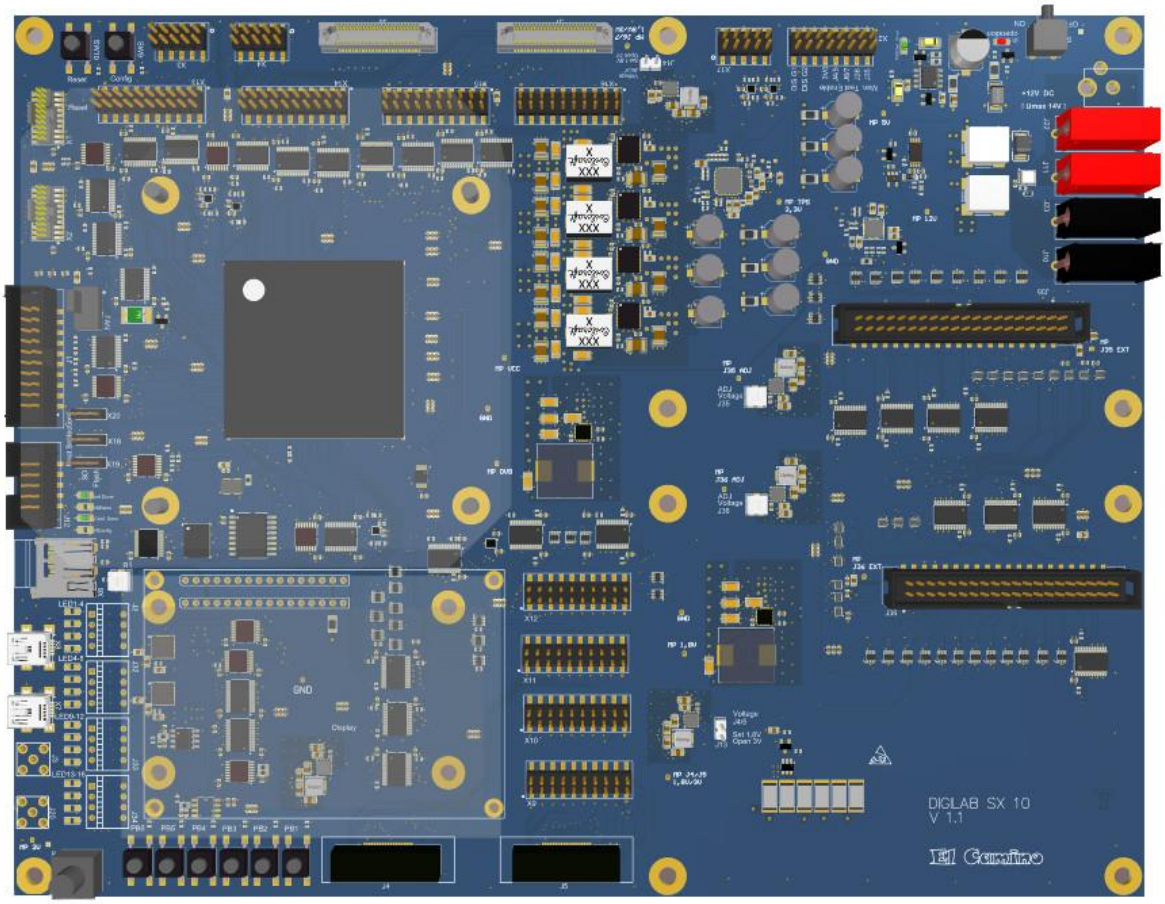
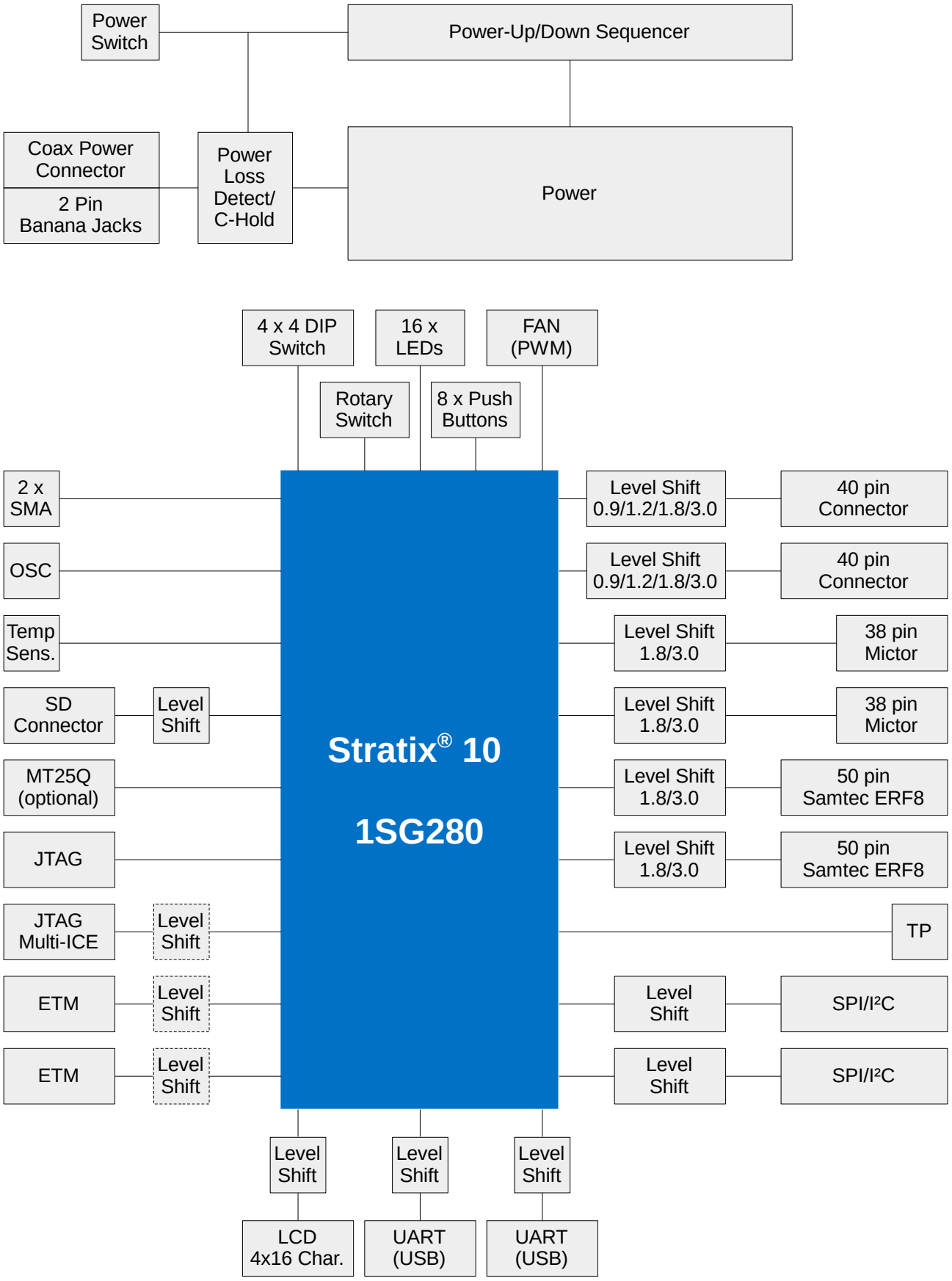


Figure 1 - DIGILAB SX 10 Block Diagram



Development Board Setup

This chapter describes how to apply power to the development board and provides default switch and jumper settings.

Setup Switches and Jumpers

Table 1 - Fundamental Board Settings

Function	Board Label	Settings	Default Position	Notes
Main Power Switch	S2		OFF	
Non-Volatile Configuration Source	X18	1-2: Boot from SD 2-3: Boot from QSPI		All three jumpers must be either set to 1-2 (configure from SD) or 2-3 (configure from QSPI)
	X19	1-2: Boot from SD 2-3: Boot from QSPI		
	X20	1-2: Boot from SD 2-3: Boot from QSPI		
Reconfigure FPGA	SW9			When pressed, triggers FPGA re-configuration (pulls nConfig low)
Mictor(J4/J5) Voltage Select	J13	Open: 3.0 V Closed: 1.8 V	Closed (1.8 V)	
Samtec (J6/J7) Voltage Select	J14	Open: 3.0 V Closed: 1.8 V	Closed (1.8 V)	
40-Pin Connector (J35) Voltage Select	R301	Poti 0.8 V – 3.0 V	0.9 V	
40-Pin Connector (J36) Voltage Select	R220	Poti 0.8 V – 3.0 V	0.9 V	
LCD Display Brightness	R1	Poti		

Board Status Information

Table 2 - Status Information

Function	Device	Color	Notes
12V/5V Present	LED17	Green	12V input voltage and 5V secondary voltage active
NCONFIG	LED18	Red	nConfig is pulled low and triggers a re-configuration of the FPGA
INIT_DONE	LED19	Green	On when INIT_DONE is driven high by the FPGA, only active when turned on in the FPGA design
CONF_DONE	LED20	Green	On when CONF_DONE output of the FPGA is released and pull-high by the external pull-up. Signals that loading configuration data into the FPGA has finished.
NSTATUS	LED22	RED	On when FPGA pulls-nStatus signal low (e.g. due to corrupt configuration data)

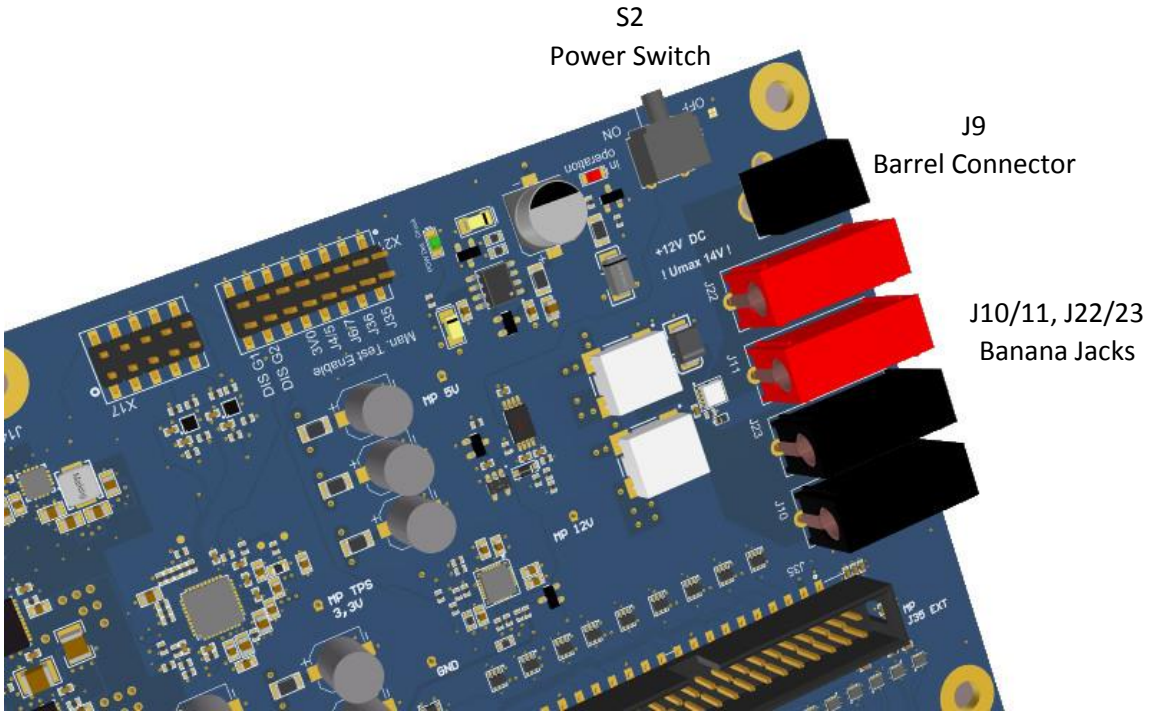
Power Up of the Board

Always use the power switch S2 to turn on and off the board.
Make sure that S2 is in the off position before you supply 12V to the board.
Turn off S2 and wait 5 seconds before turning off or disconnecting the 12V input.

The Board requires 12V/5A DC input power.

Power can be supplied through two sets of banana jacks (J10/11, J22/23) or through a barrel connector (J9).

GND	Connect GND to one or two of the black banana jacks or the outer sleeve of the barrel connector
+12V/5A DC	Connect +12V DC to one or two of the red banana jacks or to the inner tip of the barrel connector



FPGA Configuration Support

The board supports both volatile and non-volatile FPGA configuration.

Non-Volatile

Upon power-up the FPGA will try to automatically load configuration data from either an optional on-board QSPI Flash or from a pluggable SD memory card. The configuration source can be set with the jumpers X18/X19/X20 (set all jumpers to 1-2 for SD, 2-3 for QSPI).

Volatile Configuration (through JTAG)

A 10-pin standard JTAG connector (J12) can be used for volatile configuration and debugging. The supply voltage to the JTAG cable is 1.8V which is compatible e.g. with the Altera USB-Blaster or the Intel FPGA Download Cable II.

Flash Programming

The QSPI Flash, if present, can be programmed via JTAG through a JTAG indirect configuration file (JIC).
Choose the following options when converting the programming file:

- Programming file type: JTAG Indirect Configuration File (.jic)
- Configuration device: MT25QU01G
- Mode: Active Serial x4
- Flash Loader: 1SG280LN3
- SOF Data: <your .sof programming file>

The SD memory card can be prepared and programmed on a host computer.

Quartus Project

Select the following device in Quartus Prime Pro

1SG280LN3F43E3VG

This Intel Stratix 10 standard power device (–3V power grade) is a SmartVID device. A PMBus-compliant voltage regulator drives the core voltage supplies (VCC and VCCP) for this SmartVID device. The Stratix 10 device will only configure and function correctly, with appropriate Power Management & VID settings in Quartus Prime Pro.

Incorrect Power Management & VID settings in Quartus Prime can cause the voltage regulator to generate VCC and VCCP voltages above the absolute maximum ratings of the device. This can cause permanent damage or even destroy the FPGA device. One should exercise utmost care to make sure the Power Management & VID settings in Quartus Prime are correct and consistent.

The following settings are required in the Quartus Prime Gui:
Assignments – Device – Device and Pin Options – Power Management & VID

Bus speed mode	100 KHz
Slave device type	Other
PMBus device 0 slave address	71
Voltage output format	Direct format
Direct format coefficient m	100
Direct format coefficient b	-49
Direct format coefficient R	0
Translated voltage value unit	Volts

All other settings can retain its default values.

Alternatively, the following TCL commands can be used:

```
set_global_assignment -name PWRMGT_BUS_SPEED_MODE "100 KHZ"
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE OTHER
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS 71
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "DIRECT FORMAT"
set_global_assignment -name PWRMGT_DIRECT_FORMAT_COEFFICIENT_M 100
set_global_assignment -name PWRMGT_DIRECT_FORMAT_COEFFICIENT_B "-49"
set_global_assignment -name PWRMGT_DIRECT_FORMAT_COEFFICIENT_R 0
set_global_assignment -name PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS
```

Development Board Description

Clock Configuration

Figure 2 – Clocking Structure

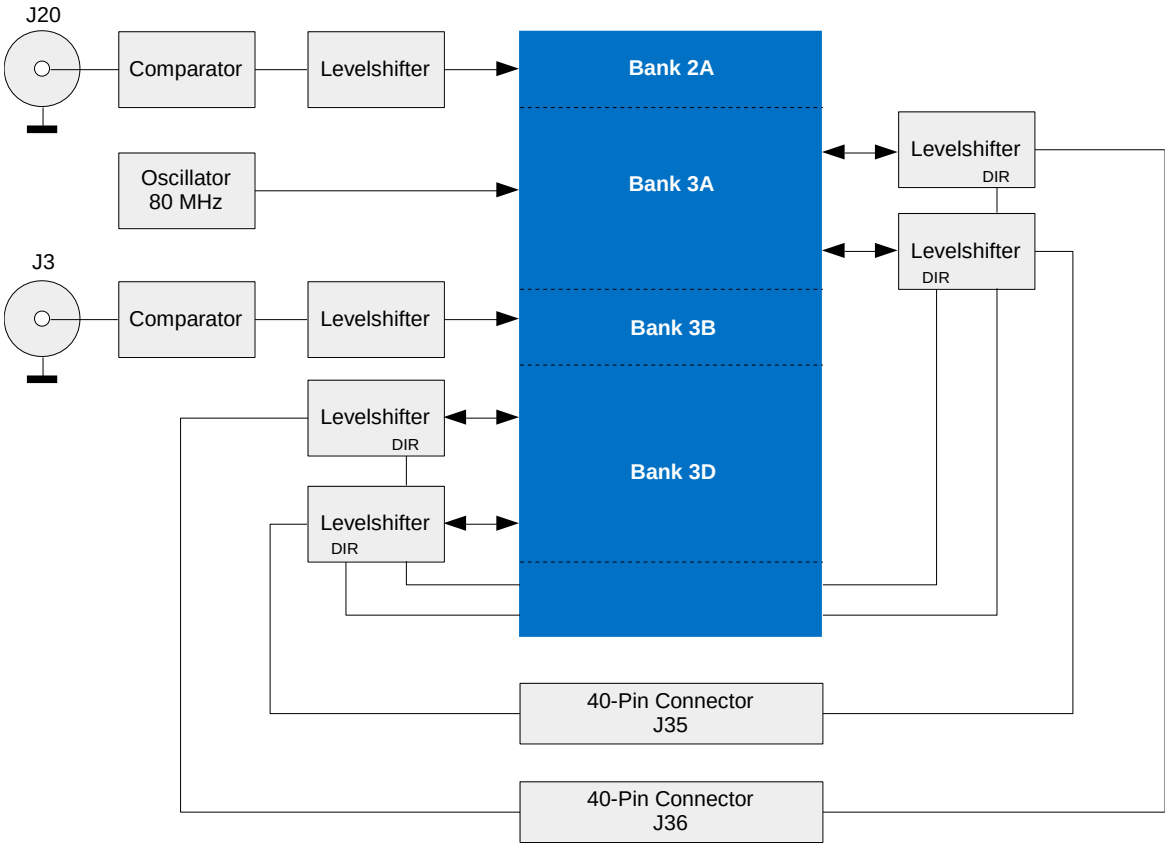


Table 3 - Clock Signals

Signal	Schematic Signal Name @ FPGA	I/O Standard @ FGPA	FPGA Pin	Notes
J20	PCLKC_IN_1	1.8V	AV27	SMA clock input connector Comparator with reference voltage @ 0.7V
J3	PCLKC_IN_2	1.8V	AL5	SMA clock input connector Comparator with reference voltage @ 0.7V
Oscillator 80 MHz	80MHz	1.8V	AV8	
J35 CLK IN	CLK_J35_IN_A_1V8	1.8V	AE6	
	CLK_J36_IN_A_DIR	1.8V	AW9	Direction control signal, ‘0’ for input
J36 CLK IN	CLK_J36_IN_A_1V8	1.8V	AD8	
	CLK_J35_IN_A_DIR	1.8V	AE6	Direction control signal, ‘0’ for input
J35 CLK OUT	CLK_TO_J35_1V8	1.8V	AV6	
	CLK_TO_J35_DIR	1.8V	AR17	Direction control signal, ‘1’ for output
J36 CLK OUT	CLK_TO_J36_1V8	1.8V	AY4	
	CLK_TO_J36_DIR	1.8V	AP29	Direction control signal, ‘1’ for output

The direction control at the level shifters for the J35/J36 clock signals is meant for when these signals are used as standard I/Os and not as clocks.

User Interface

The Development Board has the following user interface features:

- Rotary Switch
- 4 x 4 two-state DIP switches
- 7 push buttons
- 16 LEDs
- 4x16 character LCD display

Table 4 - User Interface

Function	Board Label	Schematic Signal Name @ FPGA	IO Standard @ FPGA	FPGA Pin	OFF/ IDLE	ON/ DEPRESSED
10 Position Rotary Power Switch	S1	SW_RS_1	1.8V			
		SW_RS_2	1.8V			
		SW_RS_3	1.8V			
		SW_RS_4	1.8V			
DIP Switch, 4 Positions	J2	SW_SEL1	1.8V		Pull-Up	GND
		SW_SEL2	1.8V		Pull-Up	GND
		SW_SEL3	1.8V		Pull-Up	GND
		SW_SEL4	1.8V		Pull-Up	GND
	J32	SW_SEL5	1.8V		Pull-Up	GND
		SW_SEL6	1.8V		Pull-Up	GND
		SW_SEL7	1.8V		Pull-Up	GND
		SW_SEL8	1.8V		Pull-Up	GND
	J33	SW_SEL9	1.8V		Pull-Up	GND
		SW_SEL10	1.8V		Pull-Up	GND
		SW_SEL11	1.8V		Pull-Up	GND
		SW_SEL12	1.8V		Pull-Up	GND
	J34	SW_SEL9	1.8V		Pull-Up	GND
		SW_SEL10	1.8V		Pull-Up	GND
		SW_SEL11	1.8V		Pull-Up	GND
		SW_SEL12	1.8V		Pull-Up	GND
Push Button	SW2	PB1	1.8V		Pull-Up	GND
	SW1	PB2	1.8V		Pull-Up	GND
	SW8	PB3	1.8V		Pull-Up	GND
	SW7	PB4	1.8V		Pull-Up	GND
	SW6	PB5	1.8V		Pull-Up	GND
	SW5	PB6	1.8V		Pull-Up	GND
	SW10	RESET	1.8V		Pull-Up	GND
LED	LED1	LED_1	1.8V		“0”	“1”
	LED2	LED_2	1.8V		“0”	“1”
	LED3	LED_3	1.8V		“0”	“1”
	LED4	LED_4	1.8V		“0”	“1”
	LED5	LED_5	1.8V		“0”	“1”
	LED6	LED_6	1.8V		“0”	“1”
	LED7	LED_7	1.8V		“0”	“1”
	LED8	LED_8	1.8V		“0”	“1”
	LED9	LED_9	1.8V		“0”	“1”
	LED10	LED_10	1.8V		“0”	“1”

	LED11	LED_11	1.8V		“0”	“1”
	LED12	LED_12	1.8V		“0”	“1”
	LED13	LED_13	1.8V		“0”	“1”
	LED14	LED_14	1.8V		“0”	“1”
	LED15	LED_15	1.8V		“0”	“1”
	LED16	LED_16	1.8V		“0”	“1”
LCD Display	Connector J8	LCD_RS	1.8V			
		LCD_RW	1.8V			
		LCD_EN	1.8V			
		LCD_DB_0	1.8V			
		LCD_DB_1	1.8V			
		LCD_DB_2	1.8V			
		LCD_DB_3	1.8V			
		LCD_DB_4	1.8V			
		LCD_DB_5	1.8V			
		LCD_DB_6	1.8V			
		LCD_DB_7	1.8V			

Communication Interfaces

The development board has the following communication interfaces:

- Two USB UART interface
- Two connectors for SPI/I²C interfacing

Table 5 - Communication Interfaces

Interface	Connector	Function	Schematic Signal Name @ FPGA	IO Standard @ FPGA	Direction @ FPGA	FPGA Pin
USB UART	X7	TXD	TXD_USB_X7_1V8	1.8V	In	AU25
		RTS	RTS_USB_X7_1V8	1.8V	In	AU24
		RXD	RXD_USB_X7_1V8	1.8V	Out	AC11
		CTS	CTS_USB_X7_1V8	1.8V	Out	AC10
USB UART	X8	TXD	TXD_USB_X8_1V8	1.8V	In	Y3
		RTS	RTS_USB_X8_1V8	1.8V	In	Y6
		RXD	RXD_USB_X8_1V8	1.8V	Out	AT17
		CTS	CTS_USB_X8_1V8	1.8V	Out	AT16
I2C	X3	SCL	X3_I2C_SCL_1V8	1.8V	Bidir	D5
		SDA	X3_I2C_SDA_1V8	1.8V	Bidir	C5
SPI Master		MISO	X3_SPI_MISO_1V8	1.8V	In	F1
		MOSI	X3_SPI_MOSI_1V8	1.8V	Out	E2
		CLK	X3_SPI_CLK_1V8	1.8V	Out	D1
		CS	X3_SPI_CS_1V8	1.8V	Out	D3
I2C	X4	SCL	X4_I2C_SCL_1V8	1.8V	Bidir	C7
		SDA	X4_I2C_SDA_1V8	1.8V	Bidir	E8
SPI Master		MISO	X4_SPI_MISO_1V8	1.8V	In	F2
		MOSI	X4_SPI_MOSI_1V8	1.8V	Out	A4
		CLK	X4_SPI_CLK_1V8	1.8V	Out	B5
		CS	X4_SPI_CS_1V8	1.8V	Out	A5

Connectors

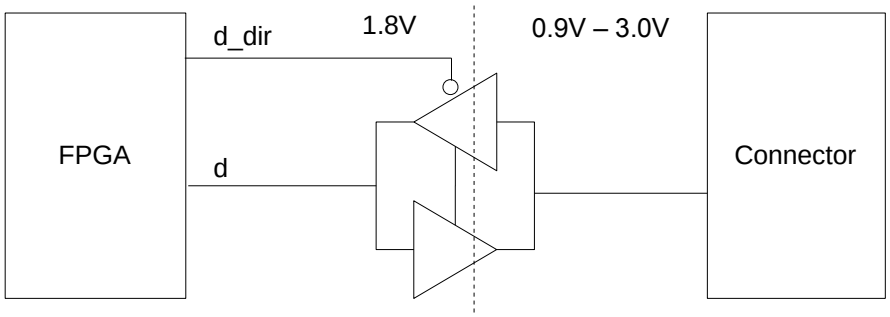
The development board has the following connectors.

- Two 40 pin DIL headers
- Two 38 pin Mictor connectors
- Two 50 pin Samtec ERF8 connectors
- Two ETM (Embedded Trace Macrocell) debug connectors
- JTAG Multi-ICE debug connector
- Shared test points

All FPGA IOs are connected through level shifters for level translation and protection. The FPGA side operates at a fixed 1.8V IO voltage. For most connectors, the voltage on the connector side can be adjusted, for some it is fixed at 3.0V.

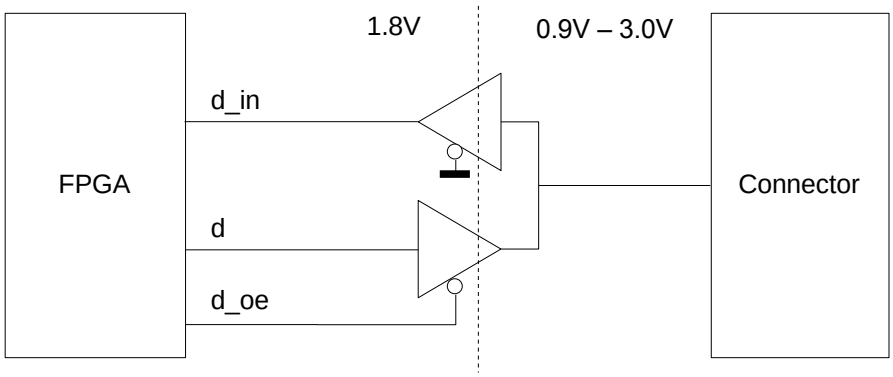
The following four types of level shifters are used:

Figure 3 - Level Shifter Type I



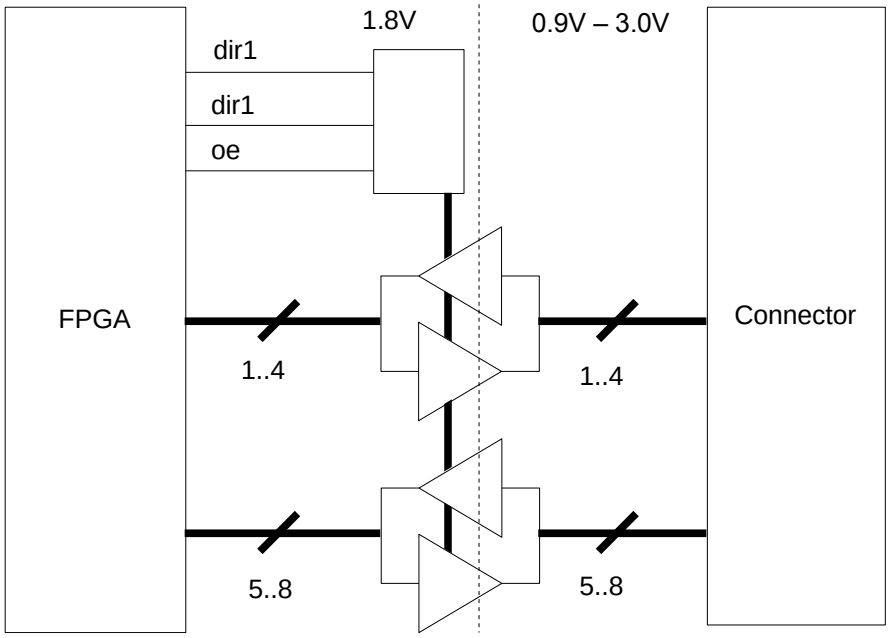
Device Type: SN74AXC1T45
Single bit configuration with direction control signal

Figure 4 - Level Shifter Type II



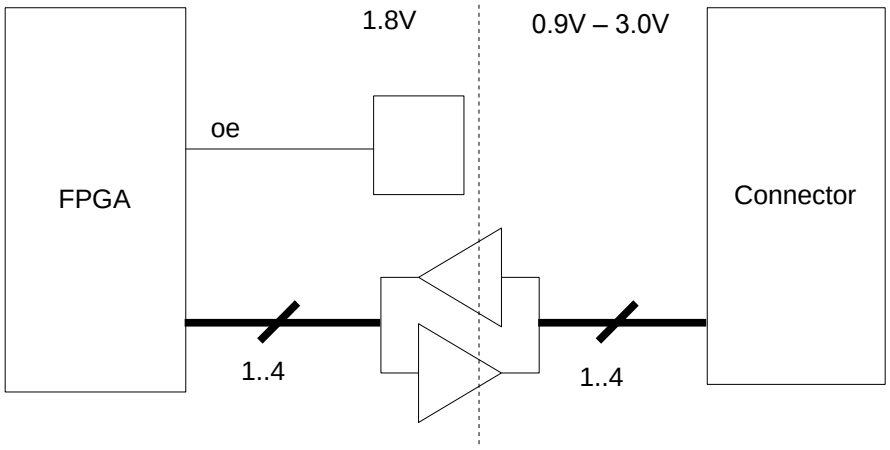
Device Type: SN74AXC1T45
Single bit with independent input and output paths.
Can be used as standard I/O or for bi-directional open drain signals like I2C.

Figure 5 - Level Shifter Type III



Device Type: SN74AXC8T245
Used to control direction of one group of 4 or two groups of 4 signals.

Figure 6 - Level Shifter Type IV



Device Type: TXB0304
4-Bit Level shifter with individual and automatic direction sensing

Table 6 - 40 Pin DIL Header J35

LS	Signal	FPGA	Signal	FPGA	Signal	FPGA	**J35**		Signal	FPGA	Signal	FPGA	Signal	FPGA	LS
					+V_J35		1	2	+V_J35_EXT						
					+V_J35		3	4	PER1CON_4	L25	PER1CON_4_EN	N26	PER1CON4_IN	K24	II
I			PER1CON_5_DIR	D13	PER1CON_5	AA9	5	6	GND						
I			CLK_J35_IN_A_DIR	K12	CLK_J35_IN_A	AE6	7	8	GND						
I			CLK_TO_J35_DIR	V7	CLK_TO_J35	AV6	9	10	PER1CON_8	G23	PER1CON_8_EN	H23	PER1CON_8_IN	H25	II
I			PER1CON_6_DIR	P6	PER1CON_6	U7	11	12	PER1CON_12	E24	PER1CON_12_EN	F24	PER1CON_12_IN	G22	II
I			PER1CON_13_DIR	P5	PER1CON_13	R6	13	14	PER1CON_15	F6	PER1CON_15_EN	E6	PER1CON_15_IN	A24	II
I			PER1CON_16_DIR	M5	PER1CON_16	P4	15	16	PER1CON_18	F7	PER1CON_18_EN	E7	PER1CON_18_IN	E9	II
					GND		17	18	PER1CON_20	T10	PER1CON_20_EN	J10	PER1CON_20_IN	G5	II
I			PER1CON_22_DIR	L6	PER1CON_22	M4	19	20	PER1CON_24	H22	PER1CON_U15_DIR1	J11	PER1CON_U15_U127_OE	F11	III
I			PER1CON_23_DIR	L7	PER1CON_23	L5	21	22	PER1CON_25	H12					III
I			PER1CON_28_DIR	J5	PER1CON_28	J4	23	24	PER1CON_30	AA11					III
					GND		25	26	PER1CON_34	L15	PER1CON_U127_DIR1	R11			III
I			PER1CON_32_DIR	U10	PER1CON_32	F4	27	28	PER1CON_38	W11					III
I			PER1CON_35_DIR	G4	PER1CON_35	H5	29	30	PER1CON_40	K13					III
I			PER1CON_37_DIR	F5	PER1CON_37	G7	31	32	PER1CON_42	V11					III
					GND		33	34	PER1CON_44	K11	PER1CON_U17_DIR1	L11	PER1CON_U17_U128_OE	H11	III
III	PER1CON_U17_U128_OE	H11	PER1CON_U128_DIR1	M22	PER1CON_46	L9	35	36	PER1CON_45	K22					III
III					PER1CON_47	L22	37	38	PER1CON_50	L12					III
III					PER1CON_54	L10	39	40	PER1CON_52	N12					III

+V_J35 Can be adjusted between 0.8V and 3.0V with Poti R301

+V_J35_EXT Is used as a connector side supply voltage for the level shifters on Pins 4 and 10 (0.65V – 3.6V)
Can be different from the common IO voltage on the connector

Table 7 - 40 Pin DIL Header J36

LS	Signal	FPGA	Signal	FPGA	Signal	FPGA	**J36**		Signal	FPGA	Signal	FPGA	Signal	FPGA	LS
					+V_J36		1	2	+V_J36_EXT						
					+V_J36		3	4	PER1CON_55	AR16	PER1CON_55_EN	AW16	PER1CON_55_IN	AN11	II
I			PER1CON_58_DIR	AU22	PER1CON_58	AP11	5	6	GND						
I			CLK_J36_IN_A_DIR	AV22	CLK_J36_IN_A	AD8	7	8	GND						
I			CLK_TO_J36_DIR	AP29	CLK_TO_J36	AY4	9	10	PER1CON_64	AW18	PER1CON_64_EN	AR17	PER1CON_64_IN	AM12	II
I			PER1CON_57_DIR	AY23	PER1CON_57	AT22	11	12	PER1CON_66	AT20	PER1CON_66_EN	AR18	PER1CON_66_IN	AT21	II
I			PER1CON_68_DIR	AY24	PER1CON_68	AU23	13	14	PER1CON_65	AP24	PER1CON_65_EN	AR21	PER1CON_65_IN	AY21	II
I			PER1CON_72_DIR	AT25	PER1CON_72	AT24	15	16	PER1CON_70	AR29	PER1CON_70_EN	AT29	PER1CON_70_IN	AD11	II
					GND		17	18	PER1CON_73	AR30	PER1CON_73_EN	AN28	PER1CON_73_IN	AN21	II
I			PER1CON_76_DIR	AT26	PER1CON_76	AW26	19	20	PER1CON_75	L29	PER1CON_U30_DIR1	AA12	PER1CON_U30_U129_OE	AM23	III
I			PER1CON_78_DIR	AU27	PER1CON_78	AR27	21	22	PER1CON_80	L30					III
I			PER1CON_82_DIR	AT31	PER1CON_82	AT30	23	24	PER1CON_84	M28					III
					GND		25	26	PER1CON_83	P30	PER1CON_U129_DIR1	N30			III
I			PER1CON_85_DIR	AM30	PER1CON_85	AN30	27	28	PER1CON_88	M30					III
I			PER1CON_90_DIR	AN25	PER1CON_90	AM28	29	30	PER1CON_92	V12					III
I			PER1CON_94_DIR	AR22	PER1CON_94	AM25	31	32	PER1CON_95	L24					III
					GND		33	34	PER1CON_98	M29	PER1CON_U32_DIR1	U12	PER1CON_U32_U130_OE	AN22	III
III	PER1CON_U32_U130_OE	AN22	PER1CON_U130_DIR1	AM24	PER1CON_97	AP23	35	36	PER1CON_100	AG12					III
III					PER1CON_104	AU12	37	38	PER1CON_102	P11					III
III					PER1CON_106	AM22	39	40	PER1CON_105	J29					III

+V_J36 Can be adjusted between 0.8V and 3.0V with Poti R220

+V_J36_EXT Is used as a connector side supply voltage for the level shifters on Pins 4 and 10 (0.65V – 3.6V)
Can be different from the common IO voltage on the connector

Table 8 - 38 Pin Mictor Connector J4

Level Shifter	Group	Signal	FPGA	Signal	FPGA	J4		Signal	FPGA	Signal	FPGA	Group	Level Shifter
				GND		1	38	GND					
				GND		2	37	GND					
IV				LA_CLK3	AT4	3	36	LA_Q1_CLK	AP5				IV
I		LA_C1_7_DIR	AU10	LA_C1_7	AR7	4	35	LA_C3_7	AM27			U57-5:8	III
III	U56-5:8			LA_C1_6	AW8	5	34	LA_C3_6	AN27			U57-5:8	III
III	U56-1:4			LA_C1_5	AM9	6	33	LA_C3_5	AP28			U57-5:8	III
III	U56-5:8			LA_C1_4	AL10	7	32	LA_C3_4	AW11	LA_C3_4_DIR	AV18		I
III	U56-5:8			LA_C1_3	AH10	8	31	LA_C3_3	AT6			U57-1:4	III
III	U56-1:4			LA_C1_2	AF11	9	30	LA_C3_2	AJ6			U57-1:4	III
III	U56-1:4			LA_C1_1	AU17	10	29	LA_C3_1	AR8			U57-1:4	III
III	U56-1:4			LA_C1_0	AV16	11	28	LA_C3_0	AY6			U57-1:4	III
III	U58-5:8			LA_C0_7	AL9	12	27	LA_C2_7	AR28			U57-5:8	III
III	U58-5:8			LA_C0_6	AK8	13	26	LA_C2_6	AP6			U58-1:4	III
III	U58-5:8			LA_C0_5	AP8	14	25	LA_C2_5	AU19	LA_C2_5_DIR	AY7		I
III	U58-5:8			LA_C0_4	AN8	15	24	LA_C2_4	AV21	LA_C2_4_DIR	AW21		I
III	U56-5:8			LA_C0_3	AF12	16	23	LA_C2_3	AE11			U58-1:4	III
III	U58-1:4			LA_C0_2	AM8	17	22	LA_C2_2	AW24	LA_C2_2_DIR			I
I		LA_C0_1_DIR	AW10	LA_C0_1	AW9	18	21	LA_C2_1	AW23	LA_C2_1_DIR			I
III	U58-1:4			LA_C0_0	AK6	19	20	LA_C2_0	AW25	LA_C2_0_DIR			I

Group		Direction 1	FPGA	Direction 2	FPGA	OE	FPGA
U56-1:4	U56-5:8	LA_C1_DIR1	AV17	LA_C1_DIR2	AM10	LA_C1_OE	AR3
U57-1:4	U57-5:8	LA_C3_DIR1	AP9	LA_C3_DIR2	AV25	LA_C3_OE	AP3
U58-1:4	U58-5:8	LA_C0_DIR1	AH8	LA_C0_DIR2	AN10	LA_C0_OE	AN7

Selectable I/O voltage - Voltage shared with connector J5
Select with jumper J13: open = 3.0 V, closed = 1.8 V

Table 9 - 38 Pin Mictor Connector J5

Level Shifter	Group	Signal	FPGA	Signal	FPGA	**J5**		Signal	FPGA	Signal	FPGA	Group	Level Shifter
				GND		1	38	GND					
				GND		2	37	GND					
IV				LA_CLK0	AT5	3	36	LA_CLK1	AR6				IV
I		LA_A3_7_DIR	AN3	LA_A3_7	AJ8	4	35	LA_A1_7	AY22			U46-5:8	III
III	U45-5:8			LA_A3_6	AD3	5	34	LA_A1_6	BB23			U46-5:8	III
III	U45-1:4			LA_A3_5	AF4	6	33	LA_A1_5	BB24			U46-5:8	III
III	U45-5:8			LA_A3_4	AE4	7	32	LA_A1_4	AM4	LA_A1_4_DIR	AP26		I
III	U45-5:8			LA_A3_3	AE3	8	31	LA_A1_3	BB25			U46-1:4	III
III	U45-1:4			LA_A3_2	AG4	9	30	LA_A1_2	BA25			U46-1:4	III
III	U45-1:4			LA_A3_1	AH3	10	29	LA_A1_1	AY26			U46-1:4	III
III	U45-1:4			LA_A3_0	AJ5	11	28	LA_A1_0	BB27			U46-1:4	III
III	U47-5:8			LA_A2_7	M9	12	27	LA_A0_7	BA24			U46-5:8	III
III	U47-5:8			LA_A2_6	V6	13	26	LA_A0_6	AA6			U47-1:4	III
III	U47-5:8			LA_A2_5	W6	14	25	LA_A0_5	AB7	LA_A0_5_DIR	AB8		I
III	U47-5:8			LA_A2_4	AA5	15	24	LA_A0_4	AB5	LA_A0_4_DIR	AC6		I
III	U45-5:8			LA_A2_3	AF5	16	23	LA_A0_3	Y7			U47-1:4	III
III	U47-1:4			LA_A2_2	AA7	17	22	LA_A0_2	AD5	LA_A0_2_DIR	AE7		I
I		LA_A2_1_DIR	AU18	LA_A2_1	AM7	18	21	LA_A0_1	AG7	LA_A0_1_DIR	AF6		I
III	U47-1:4			LA_A2_0	Y8	19	20	LA_A0_0	AL12	LA_A0_0_DIR	AP4		I

Group		Direction 1	FPGA	Direction 2	FPGA	OE	FPGA
U45-1:4	U45-5:8	LA_A3_DIR1	AK4	LA_A3_DIR2	AD4	LA_A3_OE	AK3
U46-1:4	U46-5:8	LA_A1_DIR1	AM3	LA_A1_DIR2	AL4	LA_A1_OE	BA27
U47-1:4	U47-5:8	LA_A2_DIR1	AB4	LA_A2_DIR2	P3	LA_A2_OE	AC5

Selectable I/O voltage - Voltage shared with connector J4
Select with jumper J13: open = 3.0 V, closed = 1.8 V

Table 10 - 50 Pin Samtec ERF8 Connector J6

X13	Level Shifter	Group	Signal	FPGA	J6		Signal	FPGA	Group	Level Shifter	X14
			+V_1V8_3V_J6_J7		1	2	+V_1V8_3V_J6_J7				
3	III	U61-5:8	ERF8_J6_IO_3	N1	3	4	ERF8_J6_IO_4	D15	U62-5:8	III	3
			GND		5	6	GND				
5	III	U61-5:8	ERF8_J6_IO_7	P1	7	8	ERF8_J6_IO_8	D14	U62-5:8	III	5
7	III	U61-5:8	ERF8_J6_IO_9	R2	9	10	ERF8_J6_IO_10	E13	U62-5:8	III	7
			GND		11	12	GND				
9	III	U61-5:8	ERF8_J6_IO_13	R1	13	14	ERF8_J6_IO_14	C11	U62-5:8	III	9
11	III	U61-1:4	ERF8_J6_IO_15	T2	15	16	ERF8_J6_IO_16	C10	U62-1:4	III	11
			GND		17	18	GND				
13	III	U61-1:4	ERF8_J6_IO_19	T1	19	20	ERF8_J6_IO_20	C8	U62-1:4	III	13
15	III	U61-1:4	ERF8_J6_IO_21	V2	21	22	ERF8_J6_IO_22	A7	U62-1:4	III	15
			GND		23	24	GND				
17	III	U61-1:4	ERF8_J6_IO_25	V1	25	26	ERF8_J6_IO_26	B7	U62-1:4	III	17
4	III	U63-5:8	ERF8_J6_IO_27	G2	27	28	ERF8_J6_IO_28	B25	U64-5:8	III	4
			GND		29	30	GND				
6	III	U63-5:8	ERF8_J6_IO_31	H2	31	32	ERF8_J6_IO_32	A25	U64-5:8	III	6
8	III	U63-5:8	ERF8_J6_IO_33	H1	33	34	ERF8_J6_IO_34	B24	U64-5:8	III	8
			GND		35	36	GND				
12	III	U63-5:8	ERF8_J6_IO_37	J1	37	38	ERF8_J6_IO_38	B23	U64-5:8	III	12
14	III	U63-1:4	ERF8_J6_IO_39	K2	39	40	ERF8_J6_IO_40	B22	U64-1:4	III	14
			GND		41	42	GND				
16	III	U63-1:4	ERF8_J6_IO_43	L2	43	44	ERF8_J6_IO_44	A22	U64-1:4	III	16
18	III	U63-1:4	ERF8_J6_IO_45	M2	45	46	ERF8_J6_IO_46	C21	U64-1:4	III	18
			GND		47	48	GND				
20	III	U63-1:4	ERF8_J6_IO_49	N2	49	50	ERF8_J6_IO_50	A21	U64-1:4	III	20

Group		Direction 1	FPGA	Direction 2	FPGA	OE	FPGA
U61-1:4	U61-5:8	ERF8_J6_U61_DIR1	W1	ERF8_J6_U61_DIR2	E11	ERF8_J6_U61_OE	F12
U63-1:4	U63-5:8	ERF8_J6_U63_DIR1	D11	ERF8_J6_U63_DIR2	D10	ERF8_J6_U63_OE	E12
U62-1:4	U62-5:8	ERF8_J6_U62_DIR1	A6	ERF8_J6_U62_DIR2	E16	ERF8_J6_U62_OE	G14
U64-1:4	U64-5:8	ERF8_J6_U64_DIR1	F17	ERF8_J6_U64_DIR2	T11	ERF8_J6_U64_OE	E14

Selectable I/O voltage - Voltage shared with connector J7
Select with jumper J14: open = 3.0 V, closed = 1.8 V

Table 11 - 50 Pin Samtec ERF8 Connector J7

X15	Level Shifter	Group	Signal	FPGA	J7		Signal	FPGA	Group	Level Shifter	X16
			+V_1V8_3V_J6_J7		1	2	+V_1V8_3V_J6_J7				
3	III	U65-5:8	ERF8_J7_IO_3	F21	3	4	ERF8_J7_IO_4	C26	U66-5:8	III	3
			GND		5	6	GND				
5	III	U65-5:8	ERF8_J7_IO_7	D21	7	8	ERF8_J7_IO_8	H30	U66-5:8	III	5
7	III	U65-5:8	ERF8_J7_IO_9	E21	9	10	ERF8_J7_IO_10	G27	U66-5:8	III	7
			GND		11	12	GND				
9	III	U65-5:8	ERF8_J7_IO_13	L17	13	14	ERF8_J7_IO_14	F26	U66-5:8	III	9
11	III	U65-1:4	ERF8_J7_IO_15	K17	15	16	ERF8_J7_IO_16	F27	U66-1:4	III	11
			GND		17	18	GND				
13	III	U65-1:4	ERF8_J7_IO_19	H17	19	20	ERF8_J7_IO_20	J16	U66-1:4	III	13
15	III	U65-1:4	ERF8_J7_IO_21	G17	21	22	ERF8_J7_IO_22	F25	U66-1:4	III	15
			GND		23	24	GND				
17	III	U65-1:4	ERF8_J7_IO_25	H16	25	26	ERF8_J7_IO_26	D25	U66-1:4	III	17
4	III	U67-5:8	ERF8_J7_IO_27	D26	27	28	ERF8_J7_IO_28	M25	U68-5:8	III	4
			GND		29	30	GND				
6	III	U67-5:8	ERF8_J7_IO_31	E23	31	32	ERF8_J7_IO_32	H26	U68-5:8	III	6
8	III	U67-5:8	ERF8_J7_IO_33	F16	33	34	ERF8_J7_IO_34	H27	U68-5:8	III	8
			GND		35	36	GND				
12	III	U67-5:8	ERF8_J7_IO_37	D23	37	38	ERF8_J7_IO_38	K29	U68-5:8	III	12
14	III	U67-1:4	ERF8_J7_IO_39	C23	39	40	ERF8_J7_IO_40	K30	U68-1:4	III	14
			GND		41	42	GND				
16	III	U67-1:4	ERF8_J7_IO_43	F22	43	44	ERF8_J7_IO_44	K31	U68-1:4	III	16
18	III	U67-1:4	ERF8_J7_IO_45	C22	45	46	ERF8_J7_IO_46	J30	U68-1:4	III	18
			GND		47	48	GND				
20	III	U67-1:4	ERF8_J7_IO_49	E22	49	50	ERF8_J7_IO_50	H28	U68-1:4	III	20

Group		Direction 1	FPGA	Direction 2	FPGA	OE	FPGA
U65-1:4	U65-5:8	ERF8_J6_U65_DIR1	K16	ERF8_J6_U65_DIR2	H21	ERF8_J6_U65_OE	F14
U67-1:4	U67-5:8	ERF8_J6_U67_DIR1	J21	ERF8_J6_U67_DIR2	E26	ERF8_J6_U67_OE	J23
U66-1:4	U66-5:8	ERF8_J6_U66_DIR1	C25	ERF8_J6_U66_DIR2	C27	ERF8_J6_U66_OE	D24
U68-1:4	U68-5:8	ERF8_J6_U68_DIR1	H31	ERF8_J6_U68_DIR2	N27	ERF8_J6_U68_OE	AB10

Selectable I/O voltage - Voltage shared with connector J6
Select with jumper J14: open = 3.0 V, closed = 1.8 V

Table 12 - ETM Connector X1

	Signal	FPGA	Dir	**X1 - ETM**		Signal	FPGA	Dir	Signal	FPGA	Signal	FPGA	LS
	+3V0			1	2	X1_ETM_SWDIO_TMS	J9	BIDIR	X1_ETM_SWDIO_TMS_OE	H6	X1_ETM_SWDIO_TMS_IN	AE1	II (similar)
	GND			3	4	X1_ETM_SWDCLK_TCK	AE2	IN					III (fixed)
	GND			5	6	X1_ETM_SWO_TDO_EXTA_TRACECTL	E3	OUT					III (fixed)
	OPEN			7	8	X1_ETM_NC_EXTB_TDI	AF2	IN					III (fixed)
III (fixed)	X1_ETM_TRACE_DETECT	D9	OUT	9	10	X1_ETM_NRESET	AF1	IN					III (fixed)
	OPEN			11	12	X1_ETM_TRACECLK	E4	OUT					III (fixed)
	OPEN			13	14	X1_ETM_TRACEDATA0	D4	OUT					III (fixed)
	GND			15	16	X1_ETM_TRACEDATA1	C6	OUT					III (fixed)
	GND			17	18	X1_ETM_TRACEDATA2	D6	OUT					III (fixed)
	GND			19	20	X1_ETM_TRACEDATA3	D8	OUT					III (fixed)

Table 13 - ETM Connector X2

LS	Signal	FPGA	Dir	**X2 - ETM**		Signal	FPGA	Dir	Signal	FPGA	Signal	FPGA	LS
	+3V0			1	2	X2_ETM_SWDIO_TMS	K9	BIDIR	X2_ETM_SWDIO_TMS_OE	H8	X2_ETM_SWDIO_TMS_IN	E1	II (similar)
	GND			3	4	X2_ETM_SWDCLK_TCK	AA1	IN					III (fixed)
	GND			5	6	X2_ETM_SWO_TDO_EXTA_TRACECTL	H13	OUT					III (fixed)
	OPEN			7	8	X2_ETM_NC_EXTB_TDI	AC2	IN					III (fixed)
III (fixed)	X2_ETM_TRACE_DETECT	J8	OUT	9	10	X2_ETM_NRESET	AB3	IN					III (fixed)
	OPEN			11	12	X2_ETM_TRACECLK	H3	OUT					III (fixed)
	OPEN			13	14	X2_ETM_TRACEDATA0	G12	OUT					III (fixed)
	GND			15	16	X2_ETM_TRACEDATA1	G3	OUT					III (fixed)
	GND			17	18	X2_ETM_TRACEDATA2	F10	OUT					III (fixed)
	GND			19	20	X2_ETM_TRACEDATA3	F9	OUT					III (fixed)

Table 14 - JTAG Multi-ICE Connector J1

Signal	**J1 – JTAG ICE**		Signal @ J1	FPGA	Dir	Control Signal	FPGA	Control Signal	FPGA	LS
+3V0	1	2	+3V0							
GND	3	4	ICE_TRST_N	AN2	IN					III (fixed)
GND	5	6	ICE_TDI	AM2	IN					III (fixed)
GND	7	8	ICE_TMS	AR1	BDIR	ICE_TMS_OE	AU3	ICE_TMS_IN_1V8	AL2	II (similar)
GND	9	10	ICE_TCK	AL1	IN					III (fixed)
GND	11	12	ICE_RTCK	AK1	IN					III (fixed)
GND	13	14	ICE_TDO	AR2	OUT					I (similar)
GND	15	16	ICE_SRST_N	AK2	IN					III (fixed)
GND	17	18	ICE_DBGRQ	AH2	IN					III (fixed)
GND	19	20	ICE_DBGACK	AG2	IN					III (fixed)

Additional Information

Board and User Guide Revision History

Table 15 - DIGILAB SX 10 Revision History

Date	Version	Description
November 2018	1.01	▪ Added some illustrations
November 2018	1.0	▪ Added schematic ▪ Added description for FLASH programming ▪ Added description for Quartus Prime Pro project settings and VID ▪ Added FPGA Pins in Communication Interfaces table
October 2018	0.6	Initial, Preliminary Release

Compliance and Conformity Statements

CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2004/108/EC. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

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