Advanced Optimization with Stratix 10 HyperFlex Architecture

El Camino
Training - Engineering - Consultancy

Course Description

Are you targeting a Stratix® 10 device and want to learn how your design can reach the maximum core performance?
In this course, you'll learn design techniques to enable you to unleash the full potential of the Stratix 10 HyperFlex architecture using Hyper-Optimization. You will learn how to identify logic structures that are limiting retiming and thus design performance. You will then learn how to modify your coding style and logic structures and, as a result, allow your design to achieve clock rates of up to 2 times compared to a non-optimized design, without changing overall design functionality.
Note: While the focus of this course is the Stratix 10 device family, many techniques you will learn can be used to improve performance in other device architectures.

Skills Developed

- Learn to interpret complex retiming reports to locate & understand critical chains, design paths requiring further optimization for improved performance
- Learn Hyper-Optimization techniques to restructure design logic to take advantage of the Stratix 10 HyperFlex architecture (or any FPGA architecture) using techniques such as
  - Unrolling loops
  - Pre-computation to reduce loop size
  - Shannon's Decomposition
  - Time-domain multiplexing retiming
  - Hyper-Folding
  - Loop pipelining

Skills Required

- Familiarity with FPGA/CPLD design flow
- Familiarity with the Quartus II design software
- Familiarity with Verilog or VHDL synthesizable design structures

Course Length	1 day	
Language	Presentation in German or English Slides and documentation in English	
Platform	PC, Windows 7	
Pricing	Public: Individual:	see www.elcamino.de on request
Dates	Public: Individual:	see www.elcamino.de on request

Exercises

- Loop Unrolling
  See the results of Hyper-Optimization by unrolling the loops to remove them from the design
- Shannon's Decomposition
  Practice Hyper-Optimization by using Shannon's Decomposition to reduce the amount of logic in a loop
- Hyper Folding (Manual Loop Acceleration)
  Practice Hyper-Optimization using the manual loop acceleration technique of Hyper-Folding to reduce the resource count while maintaining the system throughput

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