



## Course Description

This one-day class is a general introduction to the VHDL language and its use in logic design, covering constructs used in both the simulation and synthesis environments. By the end of this course, you will have a basic understanding of VHDL so that you can begin creating your own designs, using both behavioral and structural approaches. In the hands-on laboratory sessions, you will get to practice the knowledge you have gained by writing simple but practical designs. You will check your designs by compiling in the Quartus® II software and simulating in the ModelSim®-Altera® tool.

## Skills Developed

- Understand simulation versus synthesis environments
- Build basic VHDL models using the VHDL design units (entity, architecture, configuration, package)
- Use behavioral modeling constructs and techniques to describe logic functionality
- Use structural modeling constructs and techniques to create hierarchical designs

## Skills Required

- Background in digital logic design
- Knowledge of simulation is a plus
- Prior knowledge of a programming language (e.g., "C" language) is helpful, but not required
- No prior knowledge of VHDL or Quartus II software is needed

Course Length	1 day
Language	Presentation in German or English Slides and documentation in English
Platform	PC Windows XP / Windows 7
Pricing	On request
Dates	On request

## Exercises

- Implementing a 16-bit adder using the + operator
- Build a four input 2:1 multiplexer using IF-THEN statement
- Build a 7-segment display using CASE statement
- Build an 8-bit to 16-bit shifter using a FOR LOOP statement
- Build a 16-bit register with synchronous operation
- Build a 2 bit counter with asynchronous operation
- Examine a controlling state machine
- Build a 4x4 multiplier using LPM\_MULT
- Putting it all together by declaring and instantiating the lower-level components

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