

Interfacing to External Memory with Altera FPGAs



Course Description

You will learn to implement external memory interfaces with Altera® FPGAs & the Quartus® II software. The course provides lecture & lab exercises to help you understand the design flows, your options, & the challenges you may face. Since Double Data Rate (DDR) interfaces are most prevalent, they are the focus of the class. Nonetheless, RLDRAM II, SRAM, and QDRII/+ will also be touched upon. Through a series of lab exercises, you will learn to implement a "High Performance" DDR SDRAM controller with auto-calibrating phy block. You will also learn how to take advantage of the self-service resources available, which should improve your confidence that you can successfully complete a memory interfacing design on your own.

Skills Developed

- Understand the external memory interface options & how to choose one (eg. DDR 1, 2, 3, RLDRAM II, QDR II/+, SRAM)
- Implement the high performance DDR SDRAM controller using the MegaWizard® plug-in manager
- Verify controller functionality with the ModelSim simulator
- Close timing on your design
- Connect your own logic to the High Performance controller
- Implement multiple controllers in a single FPGA
- Learn how to use the controller within SOPC Builder

Prerequisites

We recommend completing the following courses:

- Overview of Mentor Graphic's ModelSim Software
- The Quartus II Software Design Series: Foundation (Instructor-led Training)
- The Quartus II Software Design Series: Foundation (Online Training)
- The Quartus II Software Design Series: Timing Analysis
- The Quartus II Software Design Series: Verification

Course Length	1 day
Language	Presentation in German or English Slides and documentation in English
Platform	PC Windows XP / Windows 7
Pricing	On request
Dates	On request

Skills Required

- Background in digital logic design and memory device types
- Working knowledge of the Quartus II software, especially the TimeQuest static timing analyzer
- Some knowledge of how to use a hardware simulator (eg. Mentor Graphics ModelSim® software)

Exercises

- Create Quartus II Design with High Performance DDR SDRAM Controller
- Perform Simulation of High Performance DDR Memory Controller
- Perform Timing Analysis of High Performance DDR Memory Controller
- Perform On-Board Functional Verification of High Performance Controller Using SignalTap II
- Run Memory Test on DDR or DDR2 Memory Using Nios II Processor

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