

# Best Practices for Maximizing FPGA Design Productivity



## Course Description

You will learn the best ways to maximize productivity throughout the FPGA design cycle, while also maximizing design performance. Using recommended design methodology as a framework, you will see what is involved in preparing an FPGA design and what is required to implement it - from the creation of the design specification all the way to final sign-off. Examples will be used throughout the course to provide a reference point for implementing high performance FPGA designs. These include the use of Altera devices and tools, namely Quartus® II software, for maximizing your productivity.

## Skills Developed

- Implement recommended methodologies to maximize design productivity
- Follow recommended HDL coding practices
- Start creating reusable IP
- Start performing functional verification for designs & IP using testbenches & functional coverage
- Organize a design into logical partitions to exploit incremental compilation
- Implement a plan to close timing quickly
- Implement I/O & board design in tandem with the FPGA
- Select the appropriate in-system debugging tools for the job at hand

Course Length	2 days
Language	Presentation in German or English Slides and documentation in English
Platform	PC Windows XP / Windows 7
Pricing	On request
Dates	On request

## Skills Required

- Background in digital logic design
- Basic knowledge about ASIC or programmable logic design, in particular HDL coding using VHDL or Verilog HDL

El Camino GmbH  
Landshuter Str. 1  
84048 Mainburg  
Germany

phone: +49-8751-8787-0  
fax: +49-8751-842876  
e-mail: [info@elca.de](mailto:info@elca.de)  
[www.elcamino.de](http://www.elcamino.de)

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